

CONTENTS

| | |
|---------------------------|-------|
| <i>Foreword</i> | ix |
| <i>Preface</i> | xi |
| <i>Glossary</i> | xxiii |

PART ONE FUNDAMENTALS OF INTEGRATED CIRCUIT DESIGN

| | |
|--|-----------|
| 1. Introduction to Integrated Circuits | 3 |
| 1-1 Perspective | 4 |
| Economics 5; Reliability 6; Performance 7 | |
| 1-2 Qualitative Description of Fabrication Processes | 8 |
| The Monolithic Single-crystal Approach 8; Dielectric Isolation 10; The Thin-film Approach 10; Hybrid Integrated Circuits 11 | |
| 2. Fabrication Constraints and General Design Guidelines | 12 |
| 2-1 Fabrication of a Single-crystal Monolithic Circuit | 12 |
| Photo Resist and Oxide Masking 13; Diffusion 14; Epitaxy 15; Metallization 15 | |
| 2-2 Components of Single-crystal Monolithic Circuits | 15 |
| Transistors 15; Diffused Resistors 18; Capacitors 18 | |
| 2-3 Single-crystal Monolithic Circuit Fabrication Steps | 20 |
| 2-4 Compatible Thin-film Circuits | 24 |
| 2-5 Monolithic Circuits Using Dielectric Isolation | 26 |
| 2-6 Multiple-chip Hybrid Circuits | 28 |
| 2-7 Parasitic Effects in Integrated Circuits | 29 |
| p-n Junctions 29; Diffused Resistors 29; Metal-oxide-silicon Capacitors 30; Monolithic Transistors 30; Dielectrically Isolated and Hybrid Transistors 30; Active Parasitics: Parasitic Transistor Action in Monolithic Circuits 30 | |
| 2-8 General Design Guidelines | 31 |
| Monolithic Single-crystal Circuits 31; Compatible Thin-film Techniques 32; Dielectric Isolation 32; Hybrid Circuits 32; Summary 33 | |
| 2-9 Circuit Design Guidelines | 33 |
| Monolithic Circuits 33; Hybrid Circuits 33 | |
| 2-10 Layout Design Guidelines | 34 |
| Monolithic Circuits 34; Hybrid Circuits 34 | |
| REFERENCES 35 | |
| 3. Survey of Large-signal Transistor Models | 36 |
| 3-1 Commonly Used Transistor Models | 36 |
| 3-2 The Mathematical Model | 38 |
| Basic Equations 38; Junctions 40 | |

| | | |
|-----------|--|------------|
| 3-3 | The Uniform-base Transistor | 41 |
| | The Mathematical Model 41; Regions of Operation 42; A Direct Solution for the Base Region 43 | |
| 3-4 | The Ebers-Moll Model | 45 |
| | The Active Region 45 | |
| 3-5 | The Charge-control Model | 48 |
| 3-6 | The Lumped Model | 50 |
| 3-7 | Junction Capacitances | 51 |
| 3-8 | Comparison of Models for the Uniform-base Transistor | 53 |
| 3-9 | Introduction to the Nonlinear Model | 54 |
| | REFERENCES 57 | |
| 4. | The Nonlinear Transistor Model | 58 |
| 4-1 | Introduction | 58 |
| 4-2 | Assumptions and Approximations | 60 |
| 4-3 | Analysis of the Base Region | 63 |
| | The Continuity Equation 63; The Built-in Field 64; Solution of the Con- tinuity Equation 65; The Junction Currents 65 | |
| 4-4 | Analysis of the Collector Region | 67 |
| 4-5 | The Complete Solution for the Two-junction Transistor | 68 |
| | Some Properties of the Two-junction Model 69; Short-circuit Current Gains 70 | |
| 4-6 | Simplification of the Frequency Dependence of the Transistor Model | 70 |
| | Distribution of the Poles and Zeros 71; Taylor Expansions 71; The Ap- proximate Model 72; Nature of the Approximations 74 | |
| 4-7 | Multijunction Devices | 75 |
| | The Three-junction n-p-n-p Transistor 75; The Lateral p-n-p Transistor 78 | |
| 4-8 | Frequency Dependence of the Transistor | 79 |
| 4-9 | The Piecewise Linear and Small-signal Models | 85 |
| | The Piecewise Linear Junction V-I Relations 85; The Piecewise Linear Model 88; The Small-signal Model 89; Discussion of the Piecewise Linear Model 89 | |
| 4-10 | Measurement of Nonlinear Model Parameters | 94 |
| | DC Measurements 95; Measurement of the Time Constants of the Non- linear Model 95 | |
| 4-11 | Summary | 101 |
| | REFERENCES 102 | |
| 5. | Parasitic Effects in Integrated Circuits | 103 |
| 5-1 | Junction Capacitors | 104 |
| 5-2 | Diffused Resistors | 107 |
| | Average Capacitance of the Diffused Resistor 108; Solution for the Diffused Resistor 109; Lumped Approximations for the Diffused Resistor 111 | |
| 5-3 | Metal-oxide-silicon Capacitors | 113 |
| 5-4 | Passive Parasitics of Transistors for Monolithic Single-crystal Integrated Circuits | 114 |
| | Collector Resistance 116; Substrate Resistance 122; Collector-substrate Capacitance 122; Sample Calculation of Collector Parasitics 123; Simpli- fication of the Collector Parasitic Model 126 | |
| 5-5 | Parasitics for Transistors in Hybrid and Dielectrically Isolated Integrated Circuits | 126 |

| | |
|---|------------|
| 5-6 Active Parasitics: Parasitic Transistor Action | 127 |
| 5-7 Summary | 130 |
| REFERENCES 131 | |
| | |
| PART TWO INTEGRATED LOGIC CIRCUITS | |
| 6. Terminal Parameter Characterization of Logic Circuits | 135 |
| 6-1 Logic Functions | 136 |
| 6-2 Circuit Implementation of Logic Operations | 137 |
| Emitter-coupled Logic (ECL) 137; Direct-coupled Transistor Logic (DCTL) 138; Diode-transistor Logic (DTL) 140; Transistor-transistor Logic (T^2L) 141; Memory Circuits: The Flip-flop 142 | |
| 6-3 Logic Circuit Characterization | 143 |
| DC Terminal Parameter Characterization 145; Analysis Techniques 150; Characterization of the Transient Response 151 | |
| 6-4 Performance Evaluation | 151 |
| Operating Points 151; Logic Swing, Threshold Point, Unity Gain Points, and Transition Width 154; Noise Margin, Noise Sensitivity, and Noise Immunity 154; Worst-case Characteristics 156; Power Dissipation 157; Transient Properties 157; Power-Delay Time Product 158 | |
| 6-5 Summary | 158 |
| REFERENCES 158 | |
| 7. Emitter-coupled Logic | 159 |
| 7-1 Emitter-coupled Logic Gate and Its Equivalent Circuit | 159 |
| 7-2 DC Characteristics of the ECL Gate | 162 |
| Transfer Characteristics 162; Noise Sensitivity, Noise Margins, and Transition Width 166; Worst-case Transfer Characteristics 168; Input Characteristic 171; Output Characteristics 172 | |
| 7-3 Power Dissipation | 173 |
| 7-4 Transient Analysis | 174 |
| Input Capacitance and the Base Response 175; Collector Capacitance 179; Collector Response 181; Emitter-follower Response 186 | |
| 7-5 Design Optimization | 188 |
| Total Switching Time 188; Design Equations 188 | |
| 7-6 Design Example | 191 |
| Input Capacitance (Depletion Layer Component) 191; Collector Capacitance 192; Power Division (First Iteration) 193; Parasitic Capacitance of R_{c1} and R_e (First Iteration) 193; Final Design 194; Delay Time 194 | |
| 7-7 ECL Gate Modifications | 195 |
| 7-8 Conclusions | 198 |
| REFERENCES 199 | |
| GENERAL REFERENCES 199 | |
| 8. Direct-coupled Transistor Logic | 200 |
| 8-1 Integrated DCTL Layout Considerations | 201 |
| Active Parasitics 203; Passive Parasitics 204 | |
| 8-2 Nonlinear DC Analysis of DCTL | 207 |
| Inverter Characteristics 208; DCTL Characteristics 211 | |

xviii Contents

| | | |
|------------|--|------------|
| 8-3 | Piecewise Linear Analysis | 213 |
| | General Procedure 214; Breakpoints 215; Approximations 216; Breakpoint Equations 219; Piecewise Linear Characteristics 221 | |
| 8-4 | Transient Analysis | 222 |
| | Turn-on Transient 224; Turn-off Transient 231 | |
| 8-5 | Integrated DCTL Design Considerations | 237 |
| | Logic Swing and Transition Width 238; Noise Margins 239; Worst-case Considerations 240; Maximum Fan-out 241; Power-Delay Product 245 | |
| 8-6 | Summary | 245 |
| 9. | Diode-Transistor Logic | 246 |
| 9-1 | Diodes for Integrated Circuits | 248 |
| | Multilayer Diode Configurations 249; DC Diode Characteristics 249; Parasitic Transistor Action 251; Forward Voltages 251; Diode Capacitance 255; Diode Storage Times 255; Reverse Breakdown Voltages 256; Choice of DTL Diodes 256 | |
| 9-2 | Integrated DTL Layout Considerations | 258 |
| | Active Parasitics 259; Passive Parasitics 260; Fabrication of the Input Diode Cluster 260; Additional Parasitics in the Input Cluster 264; Offset Diode, Resistor, and Transistor Parasitics 264 | |
| 9-3 | Nonlinear DC Analysis of DTL | 267 |
| 9-4 | Piecewise Linear Analysis | 272 |
| | Breakpoints 273; Approximations 273; Breakpoint Currents and Voltages 275 | |
| 9-5 | Transient Analysis | 279 |
| | Turn-on Time Constants 280; Diode and Transistor Approximations 280; Turn-on Transient 281; Turn-off Transient 283 | |
| 9-6 | DTL Design Considerations | 286 |
| | Logic Swing and Transition Width 286; Noise Margins 286; Worst-case Considerations 287; Maximum Fan-out 287; Power-Delay Product 287 | |
| 9-7 | Modification of the DTL Gate | 288 |
| 9-8 | Summary | 290 |
| | REFERENCES 290 | |
| 10. | Transistor-Transistor Logic | 291 |
| 10-1 | Integrated T ² L Layout Considerations | 291 |
| | Active Parasitics 293; Passive Parasitics 294 | |
| 10-2 | Nonlinear DC Analysis of T ² L | 294 |
| | T ² L Characteristics 294; Current Hogging in T ² L 296 | |
| 10-3 | Piecewise Linear Analysis | 301 |
| 10-4 | T ² L Transient Analysis | 305 |
| | Turn-on Transient 306; Turn-off Transient 308 | |
| 10-5 | T ² L Design Considerations | 310 |
| 10-6 | Modification of the T ² L Gate | 312 |
| 10-7 | Summary | 313 |
| 11. | Comparison of Integrated Logic Circuits | 315 |
| 11-1 | Comparison of DC Terminal Parameter Characteristics | 315 |
| | Inverse Transfer Characteristics 321 | |

| | |
|--|-----|
| 11-2 DC Transfer and Power-supply Characteristics of Monolithic Single-crystal Digital Circuits | 323 |
| 11-3 Tabulation of DC Properties | 326 |
| 11-4 Comparison of Transient Characteristics for Integrated Logic Gates | 331 |
| 11-5 Tabulation of Delay Times | 336 |
| 11-6 Noise in Integrated Digital Systems | 341 |
| Crosstalk—Lumped Parameter Approach 342; Experimental Results (Lumped Parameter Approach) 344; Crosstalk—Distributed Parameter Analysis 348; Experimental Results for the Distributed Case 351; Power-supply Noise 356; Externally Generated Noise 357 | |
| 11-7 Concluding Remarks on Digital Integrated Circuits | 360 |
| Ultrahigh Speed Range 361; High Speed Range 362; Medium Speed Range 362; Low Power Range 363 | |
| REFERENCES 364 | |

PART THREE LINEAR INTEGRATED CIRCUITS

| | |
|--|------------|
| 12. Small-signal Characterization of Integrated Transistors | 367 |
| 12-1 The Small-signal Model of the Integrated Transistor | 367 |
| Conventional Small-signal Model 368; AC Current Crowding 371; Conditions for Which AC Crowding Affects Performance 373 | |
| 12-2 Two-port Gain and Stability Functions | 374 |
| Unilateral Power Gain 375; Invariant Stability Factor 375; Maximum Frequency of Oscillation 376; Maximum Available Power Gain and Gain-stability Product 376; Available Power Gain and Transducer Gain 377 | |
| 12-3 Gain and Stability Functions of the Integrated Transistor | 379 |
| Unilateral Power Gain and Maximum Frequency of Oscillation 379; Stability Factors 382; Gain-stability Product and Maximum Available Gain 385 | |
| 12-4 Noise in Integrated Circuit Transistors | 385 |
| Integrated Transistor Noise Model 386; Single-stage Noise Figures 388; Comparison of Single-stage Noise Figures 389; Optimum Single-stage Noise Figures 391 | |
| 12-5 Noise Performance of Integrated Two-stage Cascades | 391 |
| Cascade Noise Figures 392; Optimum Cascade Noise Figures 394; Comparison of Optimum Cascade Noise Figures 395; Transformer Coupling 397 | |
| 12-6 Summary | 398 |
| REFERENCES 399 | |
| 13. DC and Differential Amplifiers | 400 |
| 13-1 Differential Amplifiers | 401 |
| 13-2 Advantages of Integrated Transistor Pairs | 402 |
| 13-3 Differential Amplifier Analysis | 403 |
| Analysis Procedure 403; Analysis of the Balanced Amplifier 405; Extension to Unbalanced Circuits 406 | |
| 13-4 Frequency Performance of the Differential Amplifier | 408 |
| 13-5 Noise in the Differential Amplifier | 409 |
| 13-6 Comparison of Integrated and Discrete Differential Amplifiers | 410 |
| 13-7 Modification of the Basic Differential Amplifier | 412 |
| 13-8 Layout Considerations | 414 |

xx Contents

| | | |
|-------------------|---|------------|
| 13-9 | Summary | 415 |
| | REFERENCES | 415 |
| 14. | High-frequency Tuned Amplifiers | 416 |
| 14-1 | Broadband Amplifier Design | 416 |
| | Noise Figure 417; Gain and Stability 418; Choice of Circuit Configuration 418; Analysis of the Cascode Stage 419; Biasing and AGC 421 | |
| 14-2 | Design of an IF Amplifier | 422 |
| | IF Stage Design 422; Layout of the IF Stage 423; Detector and Video Amplifier 424; Packaging 427; Complete IF Amplifier Assembly 427; Performance of the IF Amplifier 428 | |
| 14-3 | Narrow-band Amplifier Design | 430 |
| | Design Procedure 430; Graphical Design Procedure 433; Load Admittance 440; Input Admittance 441; The Linvill Charts 443 | |
| 14-4 | Narrow-band Amplifier Design Examples | 444 |
| | Circuit Configuration 444; Automatic Gain Control 447; Evaluation of the Small-signal Performance 447; Design of a 120-Mc Amplifier 450; Bandwidth 453; A 200-Mc Amplifier Design Example 456 | |
| 14-5 | Summary | 458 |
| | REFERENCES | 458 |
| 15. | Frequency Selective Amplification without Inductors | 460 |
| 15-1 | Active RC Networks | 461 |
| | Negative Immittance Converters 461; Gyrators 463; Networks with Controlled Sources 465 | |
| 15-2 | RC Active Networks Using Unity-gain-controlled Sources | 466 |
| 15-3 | The Digital Filter | 470 |
| 15-4 | Summary | 472 |
| | REFERENCES | 475 |
| 16. | Retrospect and Prospect | 476 |
| 16-1 | Summary | 476 |
| | DC and Low-frequency Amplifiers 477; Bandpass Amplifiers 477 | |
| 16-2 | The Impact of Integrated Circuits upon System Packaging and Design | 478 |
| | System Packaging 478; System Design 485 | |
| 16-3 | Integrated Circuit Network Theory | 485 |
| 16-4 | Theoretical Limits of the Physical Size of Microcircuits | 486 |
| 16-5 | Integrated Circuits and Neurons | 487 |
| | REFERENCES | 491 |
| APPENDIX A | Derivation of the Ebers-Moll, Charge-control, and Lumped Models | 492 |
| APPENDIX B | Common Emitter Current and Saturation Effects for Emitter-coupled Logic | 509 |
| APPENDIX C | Single Exponential Approximations for the Piecewise Linear Transient Analysis | 514 |
| APPENDIX D | Measurement Techniques for Digital Integrated Circuits | 523 |

| | |
|--|------------|
| APPENDIX E Comparison of the Cascade Noise Figures | 532 |
| APPENDIX F Controlled Sources and Nonoptimum Networks | 536 |
| <i>Index</i> | <i>541</i> |