

CONTENTS

	<i>Page</i>
I. T. HONGO: CRAY Y-MP C90 SUPERCOMPUTER	1
1. INTRODUCING THE CRAY Y-MP C90 SUPERCOMPUTER	1
2. REDEFINING HIGH-PERFORMANCE COMPUTING	1
3. BRIDGING THE GAP BETWEEN POTENTIAL AND PRODUCTIVITY ..	3
4. PROTECTING YOUR HIGH-END SUPERCOMPUTING INVESTMENTS ..	3
5. THE BEST OVERALL SUPERCOMPUTING SOLUTIONS	4
6. NEW TECHNOLOGIES MAXIMIZE SYSTEM AVAILABILITY	4
7. PHYSICAL DESCRIPTION	5
8. CRAY Y-MP C90 HIGHLIGHTS	5
9. THE MOST POWERFUL I/O TECHNOLOGY AVAILABLE	5
10. INPUT/OUTPUT HIGHLIGHTS	6
11. ADVANCED SSD TECHNOLOGY	6
12. SSD HIGHLIGHTS	7
13. DISK DRIVES	7
14. SOFTWARE	8
14.1 Performance Oriented, Feature-Rich Software	8
14.2 UNICOS Operating System	8
14.3 UNICOS Highlights	9
14.4 Compilers	10
14.5 Autotasking	10
14.6 UNICOS Storage System	11
14.7 Applications	11
14.8 The Power of Visualization	11
15. NETWORK SUPERCOMPUTING	12
15.1 Delivering Supercomputing Power to Your Desktop	12
16. SUPPORTABILITY	13
16.1 Maximized System Availability	13
17. THE CRAY Y-MP C90 SUPERCOMPUTER, NOTHING ELSE COMES CLOSE	14

II. K. UCHIDA: FUJITSU VP2000 SERIES SUPERCOMPUTER	17
1. INTRODUCTION	17
2. ARCHITECTURE	18
2.1 Scalar Unit (SU)	19
2.2 Vector Unit (VU)	19
2.3 Main Storage Unit (MSU)	20
2.4 System Storage Unit (SSU)	20
2.5 Channel Processor (CHP)	21
2.5.1 High-speed optical channel	21
2.5.2 HIPPI channel	21
3. HARDWARE IMPLEMENTATION	21
3.1 Vector Pipelines	21
3.2 Parallel Processing	22
3.3 Advanced Scalar Operation	23
3.4 Other Features for High Speed Processing	23
4. MULTIPROCESSOR SYSTEM	23
4.1 Dual Scalar Processor (DSP)	24
4.2 Quadruple Scalar Processor (QSP)	24
5. HARDWARE TECHNOLOGY	24
5.1 Advanced LSIs	24
5.2 High Density Packaging	25
5.3 Cooling Technology	25
6. MSP SYSTEM	25
6.1 System Storage Usage	25
6.1.1 High speed large scale virtual I/O	25
6.1.2 High speed swapping	26
6.2 Support of DSP/QSP	26
6.3 Virtual Machine	26
6.4 TCP/IP Support	26
7. UNIX SYSTEM	26
7.1 Optimization of Vector Processes	27
7.2 High-Speed I/O Access	27

7.3 Effective Resource Management	27
7.4 High-Speed Swapping	27
8. LANGUAGE PROCESSING SYSTEM	28
8.1 Optimization	28
8.1.1 Parallel pipeline scheduling (PPS)	28
8.1.2 Loop unrolling	28
8.2 Parallelization	28
8.2.1 Automatic parallelization	29
8.2.2 Parallelism description	29
9. PERFORMANCE	29
10. CONCLUSION	30
11. REFERENCES	30
 III. S. KAWABE: HITACHI S-820 SUPERCOMPUTER SYSTEM	43
1. INTRODUCTION	43
2. ARCHITECTURE AND SYSTEM ORGANIZATION	44
2.1 Overview	44
2.2 Extended Storage	47
2.3 Vector Register	48
2.4 Vector Instruction Set	49
3. LOGIC STRUCTURE	49
3.1 Overview	49
3.2 Vector Execution Control	51
3.2.1 Parallel construction	51
3.2.2 Elementwise parallel processing	52
3.3 Storage Control	54
4. HARDWARE TECHNOLOGY	55
5. SOFTWARE	57
6. PERFORMANCE	60
7. CONCLUSION	61
8. REFERENCES	61

IV. T. WATANABE: NEC SX-3 SUPERCOMPUTER SYSTEM	63
1. INTRODUCTION	63
2. SYSTEM CONFIGURATION	64
3. PROCESSOR CONFIGURATION AND ARCHITECTURE	64
4. THE SUPER-UX OPERATING SYSTEM	65
5. FORTRAN AND TOOLS	66
6. PERFORMANCE RESULTS	69
7. CONCLUSION	69
8. REFERENCES	70
V. K. W. NEVES: TRENDS IN VECTOR AND PARALLEL SUPERCOMPUTER ARCHITECTURES	77
1. INTRODUCTION	77
2. THE SUPERCOMPUTER CPU: AN OVERVIEW	78
3. A SUMMARY OF SUPERCOMPUTER HARDWARE CHARACTERISTICS	83
4. PARALLEL VECTOR COMPUTATION, AND LATENCY IN DESIGN ..	86
5. A STUDY OF VECTOR START-UP TIME	89
6. PARALLEL COMPUTATION	96
7. RISC ARCHITECTURES	97
8. CONCLUSION	102
9. REFERENCES	102
VI. K. FUJII, H. YOSHIHARA: NAVIER-STOKES BENCHMARK TESTS	105
1. INTRODUCTION	105
2. BENCHMARK TEST FEATURES	106
3. BENCHMARK TEST RESULT - 1	109
4. BENCHMARK TEST RESULT - 2	111

5. FINAL REMARKS ON BOTH BENCHMARK TESTS	113
5.1 Assessment of the Result	113
5.2 CFD View Point	116
6. CRAY Y-MP C-90 BENCHMARCH REPORT	117
7. FUTURE REQUIREMENTS	117
8. FINAL REMARKS	119
9. ACKNOWLEDGMENT	120
10. REFERENCES	120
 VII. W. GENTZSCH: VECTORIZATION AND PARALLELIZATION TECHNIQUES FOR MODERN SUPERCOMPUTERS	
1. INTRODUCTION	127
2. BASIC ASPECTS OF VECTOR AND PARALLEL PROCESSING	128
2.1 Vector Architectures and Vector Processing	128
2.2 Parallel Architectures and Parallel Processing	130
2.3 Shared-Memory Systems	132
2.4 Distributed-Memory Systems	132
3. VECTORIZATION AND PARALLELIZATION OF ALGORITHMS	134
3.1 Vectorization	134
3.2 Parallelization	135
3.3 Example: Restructuring of the SOR-Poisson Solver	136
3.4 Example: Vectorization of Sparse Matrix Vector Products	141
3.5 Parallelization of SOR for Shared-Memory Systems	147
3.6 Parallelization of SOR for Distributed-Memory Systems	151
3.7 Example: Numerical Grid Generation	151
4. CONCLUDING REMARKS	154

VIII. M. FUKUDA, T. IWAMIYA, H. MIYOSHI: UHSNWT INITIATIVE AT NATIONAL AEROSPACE LABORATORY	157
1. BACKGROUND OF NUMERICAL WIND TUNNEL	157
1.1 Present Situation of CFD	157
1.2 From Ultra High Speed Supercomputer to Ultra High Speed Numerical Wind Tunnel	159
2. DEMANDS IN THE SYSTEM MANAGER'S EYES	160
2.1 Costs	160
2.2 Reliability	162
3. THE UHSNWT INITIATIVE	163
3.1 Starting Point	163
3.2 Hierarchical Structure of the UHSNWT Memory	164
3.3 Required Performance – From the Manager's Viewpoints	167
3.4 Configuration of PE	169
3.4.1 Speed-up of PE	169
3.4.1.1 Pipelined vector computers with large VR	169
3.4.1.2 VTAP simulation	172
3.4.2 VTAP simulation results	173
3.4.3 PE model and its feasibility	176
3.4.4 PE models	176
3.4.5 Analysis of VTAP simulation	179
3.4.6 LSI chips for PE	183
3.5 Configuration of Main Memory	185
3.5.1 Realization of target main memory capacity	185
3.5.2 Affinity with CFD programs	187
4. OVERALL HARDWARE CONFIGURATION OF THE UHSNWT	189
4.1 Summary	189
4.2 Reliability of the UHSNWT	190
4.3 Overall Performance	191
4.4 Feasibility of UHSNWT Meeting Requirement (R2)	192
5. CONCLUDING REMARKS	192
6. REFERENCES	193
IX. ADDRESSES OF CONTRIBUTORS	199